



July 8, 1998

To: Commissioner of Patents and Trademarks

Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572

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Subject:

Serial No. 09/086,772 05/29/98

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HARD MASKING METHOD FOR FORMING PATTERNED OXYGEN CONTAINING PLASMA

ETCHABLE LAYER

| Grp. Art Unit: 1763

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

Each of these following Patents and/or Publications have been mentioned and described in the Specification of the Subject Patent Application:

- U.S. Patent 5,565,384 to Havemamm, "Self-Aligned Via Using Low Permittivity Dielectric", discloses a method where horizontal gaps between the patterned conductors are substantially filled with an organic containing dielectric material.
- U.S. Patent 5,654,240 to Lee et al, "Integrated Circuit Fabrication Having Contact Opening", shows an oxide hard mask for metal patterning.
- U.S. Patent 5,460,693 to Moslehi, "Dry Microlithography Process", shows oxide hard masks for a flourinated layer.
- U.S. Patent 5,246,883 to Lin et al, "Semiconductor Contact Via Structure And Method", shows a contact via through an IDL layer with different buffer layers.

Sincerely,

George O. Saile, Reg. No. 19572